

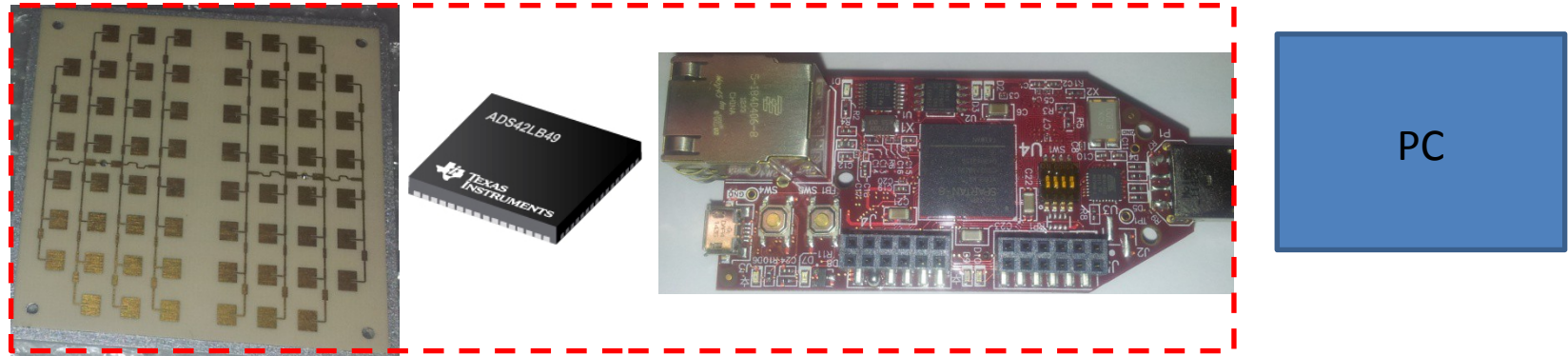
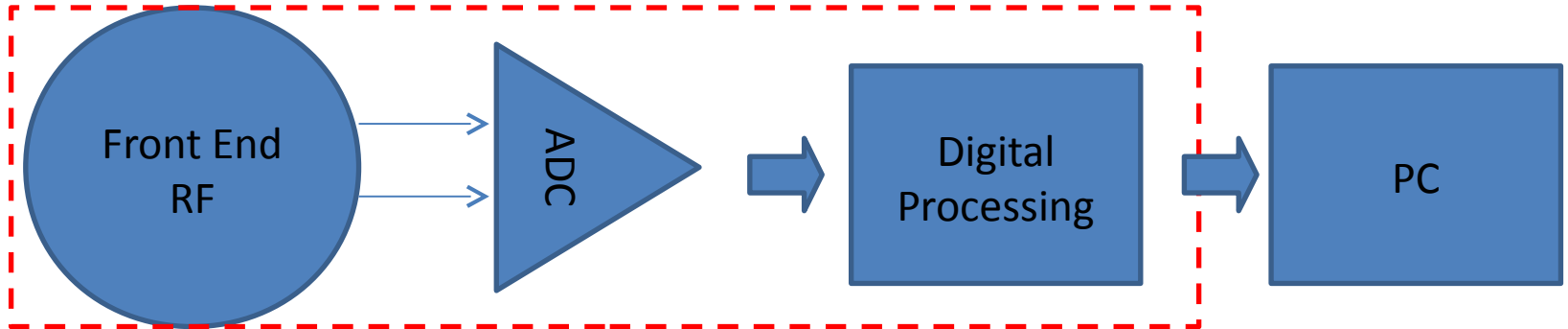


Electronic design solutions

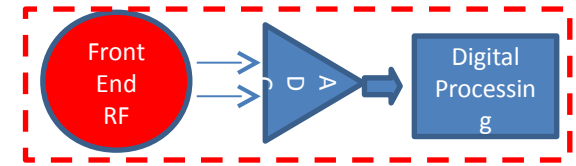
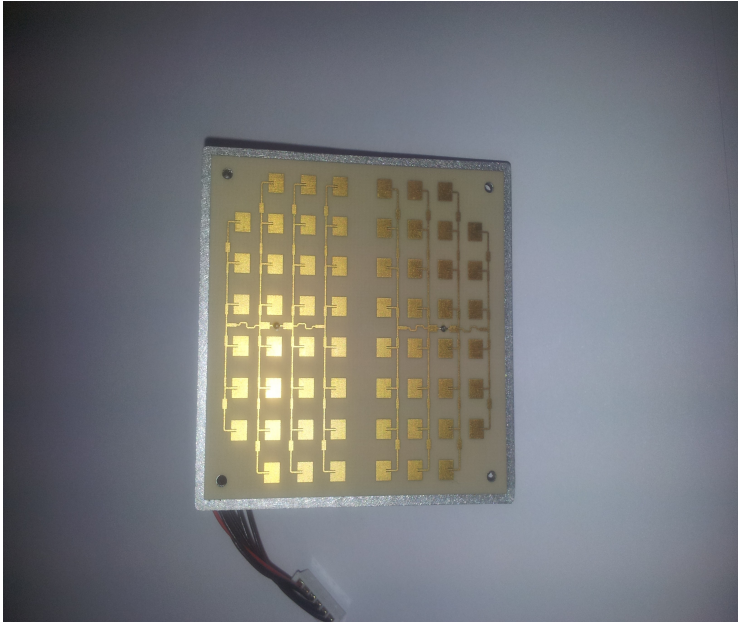
Obiettivi

1. Acquisizione di dati reali per ottimizzare modello e forme d'onda del radar ed evidenziare eventuali criticità
2. Verifica funzionalità di detezione&rivelazione di oggetti presenti al di là di un ostacolo
3. Verifica ed ottimizzazione degli algoritmi di processing digitale e di estrazione radar
4. Realizzazione specifiche HW/SW/FW per realizzare un sistema breadboard di sviluppo

Configurazione del dimostratore

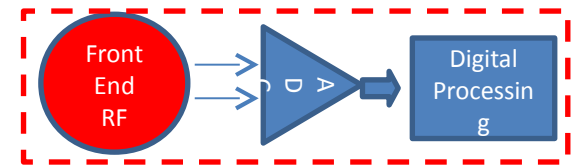


Dimostratore TTW: Sezione RF



Features:

- » VCO-Transceiver centered @ 24GHz
- » FMCW/FSK capable; therefore measurement of distance as well as recognition of stationary objects possible (depending on modulation)
- » RF-pre-amplifier for lowest noise operation
- » split transmit and receive path for maximum gain
- » stereo (dual channel) operation for direction of motion identification
- » IF-pre-amplifier, bandwidth limited for lowest noise performance
- » compact outline dimensions

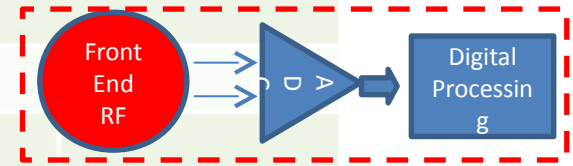


Parameter	Symbol	Min.	Typ.	Max.	Units	Comment
Oscillator						
transmit frequencies	f	24.000 - 24.250			GHz	depending on V_{tune}
varactor tuning voltage	V_{tune}	0.5		10	V	
varactor input impedance			10		k Ω	
modulation input				150	kHz	
tuning slope			50		MHz/V	
temperature drift (frequency)	Δf		-1		MHz/ $^{\circ}$ C	
output power (EIRP)	P_{out}		20		dBm	@ 25 $^{\circ}$ C

Dimostratore TTW: Sezione RF

Receiver

I/Q balance	amplitude			6	dB
	phase	60	90	120	°
IF-output	voltage offset		$V_{cc}/2$		V
IF-amplifier	bandwidth		50 - 100k		Hz
	gain		30		dB



Antenna pattern (compare with antenna plot on page 3)

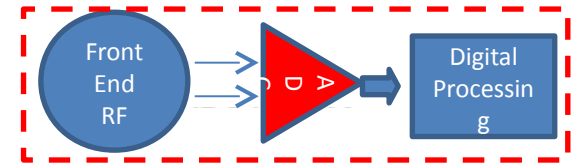
full beam width @ -3dB	horizontal		12		°	azimuth
	vertical		25		°	elevation
side-lobe suppression	horizontal		15		dB	azimuth
	vertical		15		dB	elevation

Power supply

supply voltage	V_{cc}	4.75	5.0	5.25	V	
supply current	I_{cc}		60	80	mA	IF-amp included

Environment

operating temperature	T_{op}	-20		+60	°C	
storage temperature	T_{stg}	-40		+85	°C	



Dual-Channel, 14- and 16-Bit, 250-MSPS Analog-to-Digital Converters

Check for Samples: [ADS42LB49](#), [ADS42LB69](#)

FEATURES

- Dual Channel
- 14- and 16-Bit Resolution
- Maximum Clock Rate: 250 MSPS
- Analog Input Buffer with High Impedance Input
- Flexible Input Clock Buffer with Divide-by-1, -2, and -4
- 2- V_{PP} and 2.5- V_{PP} Differential Full-Scale Input (SPI-Programmable)
- DDR or QDR LVDS Interface
- 64-Pin QFN Package (9-mm x 9-mm)
- Power Dissipation: 820 mW/ch
- Aperture Jitter: 85 fs
- Internal Dither
- Channel Isolation: 100 dB
- Performance at $f_{IN} = 170$ MHz at 2 V_{PP} , -1 dBFS
 - SNR: 73.2 dBFS

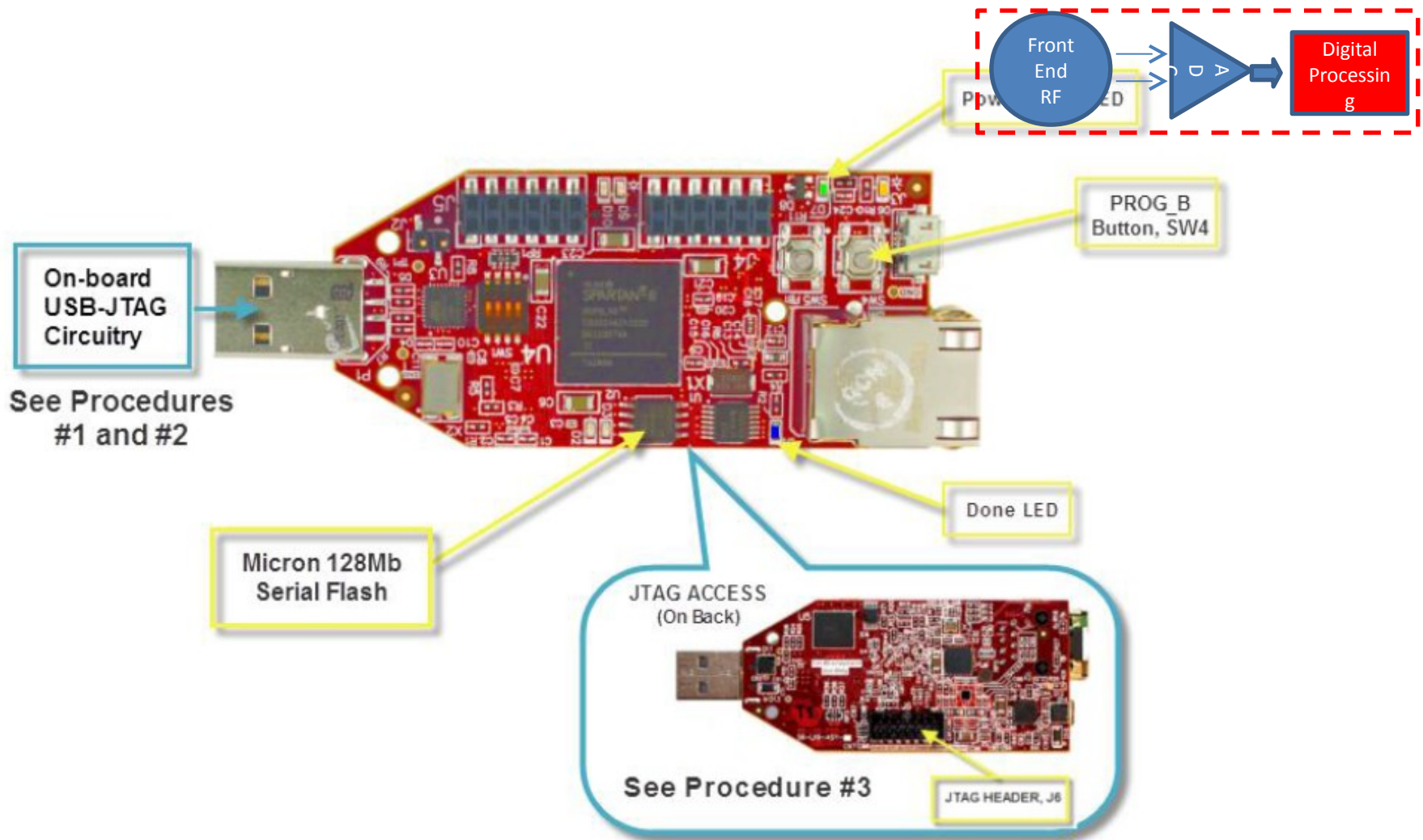
APPLICATIONS

- Communication and Cable Infrastructure
- Multi-Carrier, Multimode Cellular Receivers
- Radar and Smart Antenna Arrays
- Broadband Wireless
- Test and Measurement Systems
- Software-Defined and Diversity Radios
- Microwave and Dual-Channel I/Q Receivers
- Repeaters
- Power Amplifier Linearization

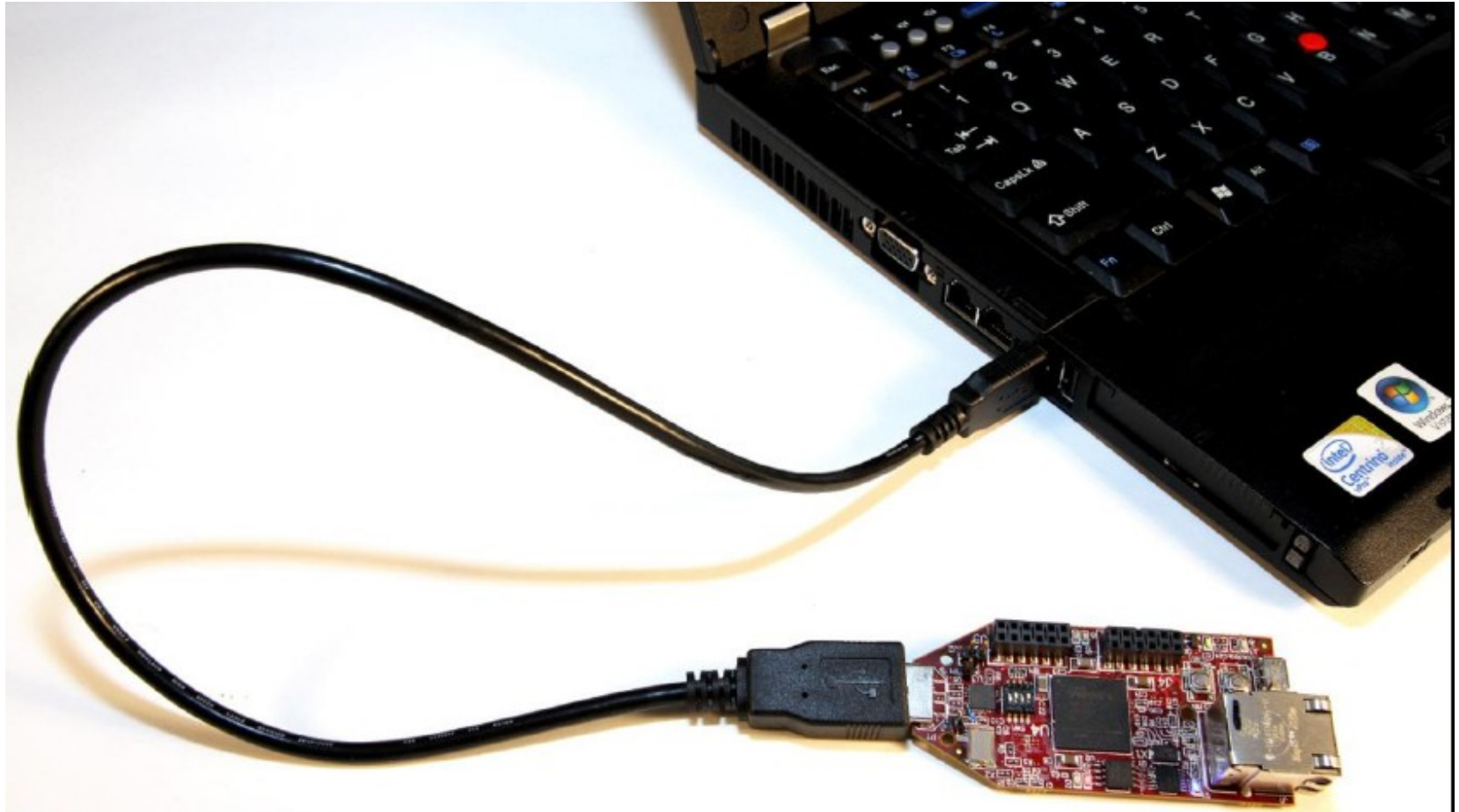
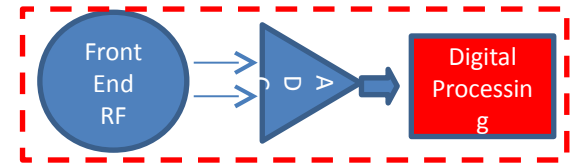


DESCRIPTION

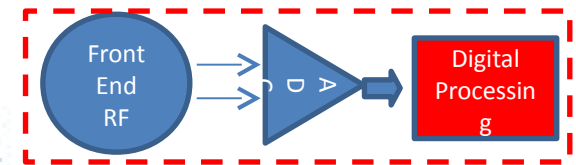
The ADS42LB49 and ADS42LB69 are a family of high-linearity, dual-channel, 14- and 16-bit, 250-MSPS, analog-to-digital converters (ADCs) supporting DDR and QDR LVDS output interfaces. The buffered analog input provides uniform input impedance across a wide frequency range while minimizing sample-and-hold glitch energy. A



Spartan-6 LX9 MicroBoard Configuration Interfaces



- Spartan-6 XC6SLX9-2CSG324C FPGA
- 64 MB LPDDR SDRAM
- 128 Mb Multi-I/O SPI Flash
- 10/100 Ethernet PHY
- USB-to-UART port
- On-board USB JTAG circuitry
- Two Digilent Pmod™ compatible headers (2x6)
- Single-chip, 3-rail power with Power Good indicator
- Programmable clock chip
- Over-voltage and ESD protection on USB
- Four LEDs
- 4-bit DIP switch
- Reset and PROG push-buttons



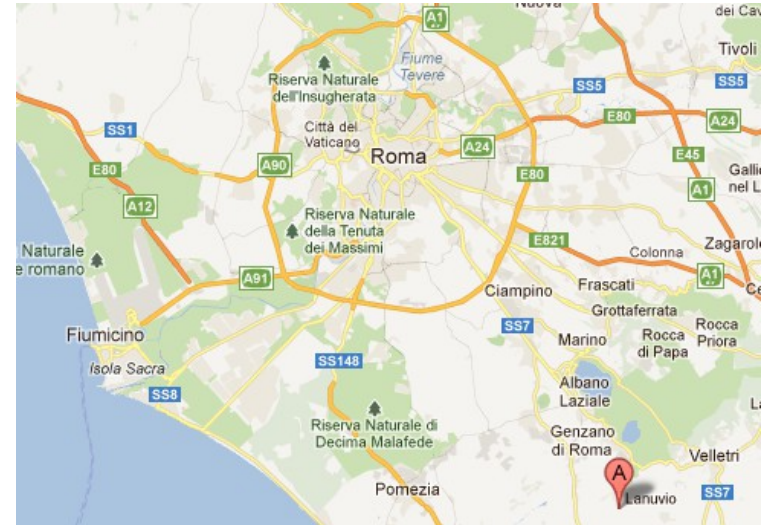
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